

CLAIMS

1. A duty ratio detecting apparatus comprising:

a duty ratio detecting circuit including first
5 and second nodes, a load current supplying circuit for
supplying first and second load currents to said first and
second nodes, respectively, and a current switch connected to
said first and second nodes, said current switch operating in
response to first and second complementary duty ratio signals;

10 a duty ratio maintaining circuit including
third and fourth nodes for receiving and maintaining voltages
at said first and second nodes, respectively;

a first switch connected between said first
and third nodes; and

15 a second switch connected between said second
and fourth nodes,

said load current supplying circuit being
controlled by voltages at said third and fourth nodes.

2. The duty ratio detecting apparatus as set forth in
20 claim 1, wherein said load current supplying circuit
comprises:

a first P-channel MOS transistor connected
between a first power supply terminal and said first node and
having a gate connected to said third node;

25 a second P-channel MOS transistor connected
between said first power supply terminal and said first node
and having a gate connected to said fourth node;

a third P-channel MOS transistor connected
between said first power supply terminal and said first node
30 and having a gate connected to said third node; and

a fourth P-channel MOS transistor connected
between said first power supply terminal and said first node
and having a gate connected to said fourth node,

said current switch comprising:

a constant current source connected to a second power supply terminal;

5 a first N-channel MOS transistor connected between said first node and said constant current source and having a gate for receiving said first complementary duty ratio signal; and

a second N-channel MOS transistor connected between said second node and said constant current source and
10 having a gate for receiving said second complementary duty ratio signal.

3. The duty ratio detecting apparatus as set forth in claim 1, wherein said load current supplying circuit comprises:

15 a first N-channel MOS transistor connected between a first power supply terminal and said first node and having a gate connected to said third node;

a second N-channel MOS transistor connected between said first power supply terminal and said first node
20 and having a gate connected to said fourth node;

a third N-channel MOS transistor connected between said first power supply terminal and said first node and having a gate connected to said third node; and

a fourth N-channel MOS transistor connected
25 between said first power supply terminal and said first node and having a gate connected to said fourth node,

said current switch comprising:

a constant current source connected to a second power supply terminal;

30 a first P-channel MOS transistor connected between said first node and said constant current source and having a gate for receiving said first complementary duty ratio signal; and

a second P-channel MOS transistor connected between said second node and said constant current source and having a gate for receiving said second complementary duty ratio signal.

5 4. The duty ratio detecting apparatus as set forth in claim 1, wherein said duty ratio maintaining circuit comprises first and second capacitors connected to said third and fourth nodes, respectively.

10 5. A duty ratio correcting apparatus for receiving and correcting an external clock signal, comprising:

a duty ratio adjusting circuit for receiving said external clock signal and adjusting a duty ratio of said external clock signal to generate an internal clock signal;

15 a differentializing circuit, connected to said duty ratio adjusting circuit, for differentializing said internal clock signal to generate first and second complementary duty ratio signals;

20 a duty ratio detecting circuit, connected to said differentializing circuit, for detecting first and second duty ratios of said first and second complementary duty ratio signals;

a switch circuit connected to said duty ratio detecting circuit; and

25 a duty ratio maintaining circuit, connected between said switch circuit and said duty ratio adjusting circuit, for maintaining said first and second duty ratios via said switch circuit as third and fourth duty ratios, respectively, so that said duty ratio adjusting circuit adjusts the duty ratio of said external clock signal in
30 accordance with said third and fourth duty ratios,

said duty ratio adjusting circuit and said differentializing circuit being deactivated by receiving a stand-by signal, said switch being opened by receiving said

stand-by signal,

said duty ratio detecting circuit comprising:
first and second nodes;

a load current supplying circuit for supplying
5 first and second load currents to said first and second nodes,
respectively; and

a current switch connected to said first and
second nodes, said current switch operating in response to
first and second complementary duty ratio signals,

10 said duty ratio maintaining circuit
comprising third and fourth nodes for receiving and
maintaining said first and second duty ratios at said first
and second nodes, respectively,

said switch circuit comprising:

15 a first switch connected between said first
and third nodes; and

a second switch connected between said second
and fourth nodes,

said load current supplying circuit being
20 controlled by said third and fourth duty ratios at said third
and fourth nodes, respectively.

6. The duty ratio correcting apparatus as set forth in
claim 5, wherein said load current supplying circuit
comprises:

25 a first P-channel MOS transistor connected
between a first power supply terminal and said first node and
having a gate connected to said third node;

a second P-channel MOS transistor connected
between said first power supply terminal and said first node
30 and having a gate connected to said fourth node;

a third P-channel MOS transistor connected
between said first power supply terminal and said first node
and having a gate connected to said third node; and

a fourth P-channel MOS transistor connected between said first power supply terminal and said first node and having a gate connected to said fourth node,

said current switch comprising:

5 a constant current source connected to a second power supply terminal;

a first N-channel MOS transistor connected between said first node and said constant current source and having a gate for receiving said first complementary duty ratio signal; and

a second N-channel MOS transistor connected between said second node and said constant current source and having a gate for receiving said second complementary duty ratio signal.

15 7. The duty ratio correcting apparatus as set forth in claim 5, wherein said load current supplying circuit comprises:

a first N-channel MOS transistor connected between a first power supply terminal and said first node and having a gate connected to said third node;

a second N-channel MOS transistor connected between said first power supply terminal and said first node and having a gate connected to said fourth node;

25 a third N-channel MOS transistor connected between said first power supply terminal and said first node and having a gate connected to said third node; and

a fourth N-channel MOS transistor connected between said first power supply terminal and said first node and having a gate connected to said fourth node,

30 said current switch comprising:

a constant current source connected to a second power supply terminal;

a first P-channel MOS transistor connected

between said first node and said constant current source and having a gate for receiving said first complementary duty ratio signal; and

5 a second P-channel MOS transistor connected between said second node and said constant current source and having a gate for receiving said second complementary duty ratio signal.

8. The duty ratio correcting apparatus as set forth in claim 5, wherein said duty ratio maintaining circuit comprises
10 first and second capacitors connected to said third and fourth nodes, respectively.